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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,426	06/19/2001	Daniel Sobek	AMD-E306	4225

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EXAMINER	
VU, QUANG D	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,426	SOBEK ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16-18, 21, 22, 26, 27, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,859,454 to Choi et al. in view of US Patent No. 5,739,569 to Chen and US Patent No. 5,879,990 to Dormans et al.

Regarding claim 16, Choi (figures 4-12) teaches a process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate (21) above the channel of the substrate (40);

forming bit lines (31) on both sides of the gate (21) subsequent to the forming the gate.

Choi et al. differ from the claimed invention by not showing the polysilicon gate. However, Chen (figures 10a-c) teaches the polysilicon gate (column 6, lines 36-39, lines 49-51). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chen into the method taught by Choi et al. because the polysilicon is a known material for the gate.

Choi et al. and Chen differ form the claimed invention by not siliciding the bitlines. However, Dormans et al. (figures 7-8) teach siliciding layer (26) (column 5, lines 21-27).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into the method taught by Choi et al. and Chen because the silicide layer reduces the resistivity of the bitlines.

Regarding claim 17, Choi et al. and Chen differ from the claimed invention by not showing siliciding the polysilicon layer. However, Dormans et al. (figures 7-8) teach siliciding the polysilicon layer (21) (column 5, lines 21-27). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into the method taught by Choi et al. and Chen because the silicide layer reduce the resistivity of the polysilicon gate.

Regarding claim 18, the combined device shows the siliciding of the bitlines and the polysilicon layer occur simultaneously (Dormans et al.; column 5, lines 21-27).

Regarding claim 21, Choi et al. and Chen differ form the claimed invention by not showing the gate comprises an N-type material. However, Dormans et al. teach the gate layer (17) comprises an N-type material (column 4, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into the method taught by Choi et al., Chen because it reduces the resistance of the gate electrode.

Regarding claim 22, Choi et al. and Chen differ from the claimed invention by not showing the gate comprises a polycrystalline silicon. However, Dormans et al. teach the gate comprises a polycrystalline silicon (column 4, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate

the teaching of Dormans et al. into method taught by Choi et al. and Chen, since it is a conventional gate electrode material.

Regarding claim 26, the combined device shows the memory cell comprises an EEPROM memory cell (Chen; column 1, lines 39-40).

Regarding claim 27, the combined device shows the memory cell comprises a two-bit memory cell (Choi et al.; column 1, lines 28-32).

Regarding claim 29, the combined device differs from the claimed invention by not showing the process further comprising scaling the length of the bitlines. It would have been ordinary skill in the art at the time the invention was made to scale the length of the bitlines because it fits the bit line into the device. Furthermore, it has been held that discovering an optimum value of a result effect variable involves only routine skill the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The length of the bitline also depends on the density of the memory device.

Regarding claim 30, the combined device differs from the claimed invention by not showing the scaling comprises reducing the thermal cycle of the bitlines. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the bitlines by thermal process because it reduces or increases the length of the bitline.

3. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. and Chen in view of Dormans et al., and further in view of US Patent No. 5,942,782 to Hsu.

Regarding claim 15, the disclosures of Choi et al., Chen and Dormans et al. are discussed as applied to claims 16-18, 21, 22, 26, 27, 29 and 30 above.

The combined device differs from the claimed invention by not showing forming an oxide over the silicided bitline. However, Hsu (figures 2A-F) teaches forming an oxide layer (34). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hsu into the method taught by Choi et al., Chen and Dormans et al. because it protects the device from the external damage. The combined device shows forming an oxide over the silicided bitline.

4. Claims 19-20 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. and Chen in view of Dormans et al., and further in view of US Patent No. 6,218,695 to Nachumovsky.

The disclosures of Choi et al., Chen and Dormans et al. are discussed as applied to claims 16-18, 21, 22, 26, 27, 29 and 30 above.

Regarding claim 19, Choi et al. differ from the claimed invention by not showing ONO layer. However, Chen (figure 10a-c) teaches the ONO layer (115, 116, 118). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chen into the method taught by Choi et al. because of the well-known advantages such as high dielectric constant of ONO.

Choi et al. and Chen differ from the claimed invention by not showing forming a charge-trapping region that contains a first amount of charge. However, Nachumovsky (figure 1) teaches forming a charge-trapping region that contains a first amount of charge (electron jump into the nitride layer [20] by hot electron injection; column 1, lines 25-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

incorporate the teaching of Nachumovsky into the method taught by Choi et al. and Chen because it stores the electron in the nitride layer. The combined device shows forming a charge-trapping region that contains a first amount of charge.

The combined device shows forming a layer (Chen; 115) between the channel and the charge-trapping region (Chen; 116). The combined device differs from the claimed invention by not showing the layer has a thickness such that the first amount of charge is prevented from directly tunneling into the layer. It is inherent that the first amount of charge is prevented from directly tunneling into the layer because the first amount of charge (electron) jumps into the charge storage region by hot electron injection.

Regarding claim 20, the combined device shows the charge trapping region (Chen; nitride layer [116]) comprises silicon nitride (Chen; column 6, lines 30-32).

Regarding claim 23, the combined device forming an insulating layer (Chen; 118) on the charge-trapping region (Chen; 116).

Regarding claim 24, the combined device shows the insulating layer (Chen; 118) comprises silicon oxide (Chen; column 6, lines 33-35).

Regarding claim 25, the combined device shows the charge trapping region (Chen; 116) comprises silicon nitride (Chen; column 6, lines 30-32).

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al. and Chen in view of Dormans et al., and further in view of US Patent No. 6,477,084 to Eitan.

Regarding claim 28, the disclosures of Choi et al., Chen and Dormans et al. are discussed as applied to claims 16-18, 21, 22, 26, 27, 29 and 30 above.

The combined device differs from the claimed invention by not showing a p-type substrate. However, Eitan teaches the substrate comprises a p-type substrate (column 8, lines 1-3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Eitan into the method taught by Choi et al., Chen and Dormans et al. because it is a known semiconductor material for substrate.

Response to Arguments

Applicant's arguments with respect to claims 15-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
September 24, 2004

DONGHEE KANG
PRIMARY EXAMINER